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Arrangement for securing control information, coupled with the memory entries of a main memory, in a multiprocessor system.

Multiple storage of the control bit (EX) indicating the exclusive responsibility via the main memory or one of the cache memories and evaluation by means of majority decision elements (MCH1) coupled with the securement of the designation bit (CA-KB) or with multiple storage of the address bits (BO to B2) of the address (CA-AD) of the relevant cache memory and monitoring by means of majority decision elements (MCH2 to MCH4). With up to eight cache memories, a control information system consisting of 12 bits is optimal, where a triple storage and/or a securing of individual designation bits (CA-KB) by a parity bit (P) as check character (SZ) renders 1-bit-errors harmless and prevents data inconsistencies.

Description

The invention concerns an arrangement in accordance with the generic term of the Patent Claim 1.

In a multiprocessor system with cache memories, special precautionary measures have to be made in order to maintain data consistency because altered data, which one of the processors wants to access, are not always available in the main memory but are available instead in one of the cache memories, or because some data to be altered by a processor may also be entered in another cache memory. In the one case, the main memory must know in which cache memory the data are available, and in the other case, the data entered in other cache memories are to be declared invalid.

For this purpose, it is a known method to couple the memory entries in the main memory or in the memory units forming the main memory with additional control information which, on the one hand, indicate whether the main memory or one of the cache memories bears the exclusive responsibility for the relevant memory entry. If it is a cache memory, then its address is additionally stated. If, otherwise, it is the main memory, then there is an additional indication as to which one of the cache memories contains the relevant entry so that the marked cache memories can be targeted and activated in order to declare the entries invalid if and when another cache memory wants to take over the responsibility exclusively.

This control information can be stored immediately together with the respective memory entry in the main memory and/or its memory units or in special tables – refer to, for example, the Conference Proceedings of the 14th Annual International Symposium on Computer Architecture, 1987, pages 234 to 243, in particular Section 5.

The control information in this case consists of one control bit which, for example, with the value "0" indicates the responsibility via the main memory and with the value "1" the responsibility via one of the cache memories, whose address is entered in a subsequently arranged memory area. For the designation of the individual cache memories, having same-addressed memory entries, this subsequently arranged memory area can consist at the same time of a number of bits corresponding to the number of the cache memories, of which one is individually allocated to one of the cache memories in each case.

This mode of control information allows an extremely quick decision on the question as to where the desired data are available and if, as required, entries in other cache memories and in which cache memories are to be declared invalid. On the other hand, control sequences dependent on individual control bits are very susceptible to disturbance, particularly with the use of high-integrated memory elements for the storage. In this way, for example, an error in the control bit for the responsibility of a memory entry or with the designation bits for the cache memories would lead very quickly to a data inconsistency in the system.

It is therefore the task assignment of the invention to alter the control information and its evaluation for the control sequence in such a way that, in an uncomplicated manner, a higher degree of security is established and faulty control sequences leading to data inconsistency are avoided.

Proceeding on the basis of an arrangement according to the generic term of the Patent Claim 1, this task assignment is solved by the characterising features of the Patent Claim 1.

Accordingly, the customary formation of a uniform check character for the entire control information is exited and the securing is effected separately in various combinations depending on the significance of contents of the control information. In every case the control bit is therefore always multiply stored so that a majority decision ensuring a greater degree of security can be taken. With a triple storage, for example, a one-bit-error does not cause a faulty control sequence because this is recognised without any problems and corrected without complexity. The same applies in the case of a multiple storage of the address bits in the subsequently arranged memory area. In the other case, and for the same degree of security, it is sufficient when a one-bit-error is recognised because, as a result of a substitution-effected designation of all cache memories existing in the system according to a further formation, a control sequence leading to data inconsistency can also be avoided even if, as the case may be, several cache memories are called up unnecessarily for the invalidity declaration of entered data. If one wants to avoid these, then, for example, another check character which will make a correction possible must be established instead of one single parity bit.

With the use of individual designation bits, the number of the required designation bits with regard to the securing bits necessary for a required degree of security does not normally coincide with the number of required memory bits for a similar security degree by means of a multiplication of the address bits. Optimal utilisation of the memory bits for both storage modes exists therefore in only a few cases, so that numerous individual bits remain unused in the one or in the other storage mode. With reference to a one-bit-error recognition for the designation bits and a one-bit-error correction for the address bits, the optimum lies in the region of nine memory bits which are used in one case for eight designation bits and one parity bit and, in the other case, for a threefold storage of the address bits.

For a better utilisation of the memory bits with a pre-specified degree of security, it can therefore be purposeful to allocate to a part of the available memory bits, in each case, several cache memories to be designated and to use the available remaining part for controlling the allocation to the individual relevant cache memories. For example, of the existing 16 cache memories, two in each case can be allocated to a designation bit where three additional control bits indicate whether, in the given case, only the first or only the second or even both cache memories can be regarded as designated whereas the security is effected by means of one single parity bit. This results in a total of 12 memory bits which, on the other hand, can be used for a triple storage of the total of four address bits.

Details of the invention will be better understood on the basis of a most preferred embodiment as shown in the drawing.

The individual details are as follows:

Fig. 1: a structural illustration of a multiprocessor system
Fig. 2: an example for a structural arrangement of the control information according to the invention in the table memories of **Fig. 1**, and
Fig. 3: a block diagram of a part of the control circuit belonging to a table memory of **Fig. 1.**

Fig. 1 shows the known structure of a multiprocessor system with a common main memory which is subdivided into several memory units M..., to which the processors P... with pre-connected cache memory STC... and SIC... have access via a connecting network VN. The cache memories in each case have a two-stage design, of which one memory STC ... works with through-storage of altered data and the second SIC... collects the altered data until a return storage into the main memory is necessary so that the connecting network VN, in the known mode, is only loaded in a case of request.
To each memory unit M..., a table memory DIR... addressable in the same manner is allocated for the control information coupled with every memory entry in the relevant memory unit.
The structural arrangement of such a control information can be seen in **Fig. 2**. For each entry, 12 bits BIT0 to BIT11 are envisaged. The first three bits refer to the control bit EX which is stored threefold and with the value "0" of the exclusive responsibility via the main memory as well as with the value "1" designates the exclusive responsibility via one of the cache memories SIC/STC. At the value "0", the subsequent eight bits as individual designating bits CA-KB designate eight different cache memories, whereas the last bit is a parity bit which as a check character SZ secures the eight designation bits so that a one-bit error is recognisable. At the value "1", for the control bit EX, the remaining nine memory bits indicate, in each case, the threefold stored address bits B0 to B2 of the address CA – AD of the relevant cache memory.
If there are less than eight cache memories in the system, the non-required designation bits CA-KB are simply set to the value "0". If more than eight cache memories are to be taken into consideration, then the entry is extended accordingly where, in the case of an allocation with a cache address CA-AD the additional memory bits remain unused, if – as already explained – one does not want to move over to a multiple designation or change over to another security degree if the number of the cache memories to be monitored is more favourable for this purpose.
Fig. 3 shows a block diagram, with reference to the structural arrangement of the control information of **Fig. 2**, of the table memory with the concerned part of the relevant control. The entry from the memory part DIR-SP based on the address MAD and taken over in each case into the read register LREG is checked on the one hand by the majority decision function MCH1 to MCH4 and, on the other hand, by the check unit SZCH with regard to the designation bits CA-KB. If the majority decision function MCH1 delivers a set control bit EX and, consequently, a request signal REQ_{COH} for the activation of the cache memory bearing the exclusive responsibility for the relevant memory entry, then the address $CA\text{-}AD_{COH}$ delivered by the majority decision functions MCH2 to MCH4 is released by the selective switch SEL1 as address $CA\text{-}AD_E$ of the cache memory to be activated for continued control at its outlet.

In the other case, and by way of the selective switch SEL2, the read designation bits CA-KB, if no error ERR is detected by the check unit SZCH, are switched through to the control UP-ST, which in successive order determines the relevant address $CA\text{-}AD_{UP}$ to each set designation bit CA-KB, which is then released via the selective switch SEL1 for the activation of the relevant cache memory. A request signal REQ_{UP} transmitted from the control UP-ST parallel in each case indicates that an entry designated by the co-delivered memory address MAD is to be declared invalid.
If the check unit SZCH detects an error ERR, then the content CA-KB′ from the register CONFR, instead of the designation bits CA-KB, is switched through via the selective switch SEL2 to the control UP-ST. For each cache memory existing in the system, the register indicates a set designation bit so that, in the event of any error as well as in order to be on the safe side, all cache memories are activated in successive order for the invalidity declaration of an addressed memory entry.
With each storage request, which leads to the reading of the relevant control information from the memory part DIR-SP, a new control information entry must be established. This is effected by the control part shown in the upper part of **Fig. 3**, dependent on the address $CA\text{-}AD_S$ of the requesting cache memory and the mode of request according to the following scheme.

Mode of memory request	Read control bit EX	Generated control signal	Sequence
Reading by cache memory without write authorisation	1	SELAD0	Delete old control information and set CA-KB for requesting cache memory
	0	SELAD1	Insert CA-KB for requesting cache memory into read control information
Updating request from one cache memory	0	SELAD2	Deletion of the relevant CA-KB in the read control information
	1	---	Error
Return write from a cache memory or a processor without cache memory	1	JNH	Deletion of the read control information
	0	---	Error
Reading by cache memory with write authorisation	X	RDMSB	Set control bit EX and enter address $CA\text{-}AD_S$ of the requesting cache memory

The derivation of the resulting control signals is not shown separately in **Fig. 3.** Only the control part influenced in the process is shown. In this, the address CA-AD_S of the respective requesting cache memory is coded, of the one input group 1 of a selective switch SEL3 which is set in dependence of the control signal RDMSB and, on the other hand, led to a decoder DEC which delivers a "1" out of n''-marking for the respectively relevant designation bit CA-KB. This marking is conducted either direct to one of the three inputs of a further selective switch SEL4 or, by way of an OR-Switch OR for mixing with the designation bits of the read control information, or to an AND element group U for deleting the marked designation bits in the read control information.
The output of this selective switch SEL4 is coupled with a security generator SZG which delivers the check character SZ in the form of a parity bit P for the eight designation bits CA-KB. The designation bits together with the established check character SZ are conducted to the other input group 0 of the selective switch SEL3. Both input groups 0 and 1 of the selective switch are supplemented by three inputs on a fixed potential which deliver the relevant control bit EX in each case, so that, with this selective switch SEL3 the bit combination representing the new control information for storage in the memory part DIR-SP is made available.

Patent Claims

1. Arrangement for securing control information, coupled with the memory entries of a main memory (memory units M...), in a multiprocessor system, where individual cache memories (STC/SIC...) are allocated to several or all processors, in which case the control information to each memory entry designates whether, for this memory entry, the main memory (e.g. memory unit M1) or a designated cache memory (e.g. SICn/STCn) is responsible or, in the event of exclusive responsibility of the main memory, this memory entry is additionally and simultaneously entered in one or several of the cache memories designated by control bits and, subsequently, in the event of a reading request with write authorisation to the main memory, the data in the designated cache memories are to be declared invalid,
thus characterised,
that, instead of a control bit (EX) for the designation of the exclusive responsibility, several (e.g. 3) bit positions (BIT0 to BIT2) of the control information are used, into which the same binary value ("0" or "1") is entered, respectively, and which are evaluated together by a majority decision element (MCH1),
that, in addition to the required n bit positions for the designation bits (CA-KB) for the designation of the cache memories (SICn/STCn), further bit positions for securing the designation bits are envisaged which, with the exclusive responsibility of the main memory for the relevant memory entry, secure the designation bits (CA-KB),
that, with exclusive responsibility of one of the cache memories (SIC.../STC...), the values of the individual bit positions (e.g. B0 to B2) of the respective cache address (CA-AD) consisting of 1d (e.g. three) bit positions are each multiply stored in the existing n+m bit or a part thereof, and the multiply stored values of a bit position are each evaluated by a majority decision element (MCH2 to MCH4) and
that, depending on the evaluation of the bit positions for the control bit (EX), either the cache address (CA-AD_{COH}) delivered by the majority decision elements (MCH2 to MCH4) for the cache address bits (B0 to B2), or a cache address (CA-AD_{UP}) derived from the individual designation bits (CA-KB) is released for the further control mode upon error-free designation (ERR=0).

2. Arrangement according to Claim 1, thus characterised, that in the event of a faulty storage (ERR=1) of the designation bits (CA-KB) for the further control mode and the derivation of the respective new information, the designation bits (CA-KB´) are set for all cache memories (SIC.../STC...) existing in the system.

3. Arrangement according to Claim 1 or Claim 2, thus characterised that the designation bits (CA-KB) are individually allocated to the cache memories (SICn/STCn).

4. Arrangement according to Claim 3, thus characterised that, with up to a maximum of eight cache memories in the system, the control information consists of twelve bits (BIT0 to BIT11), of which three bits (BIT0 to BIT2) are used for the multiple storage of the control bit (EX), whereas in one case the remaining nine bits (BIT3 to BIT11) are allocated to the eight designation bits (CA-KB) for the cache memories (CA) and a common parity bit (P) as a check character (SZ) and, in the other case, to the respective tripled three address bits (B0 to B2) of the individual cache address (CA-AD).

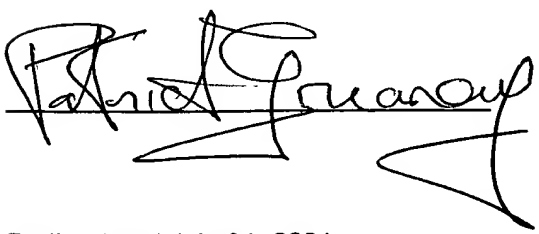
5. Arrangement according to Claim 1 or Claim 2, thus characterised that a part of the designation bits is allocated simultaneously to several (e.g. two) cache memories, and a further part of the designation bits controls the allocation of the multiple-used designation bits to the individual cache memories.

- 2 page(s) of drawings attached hereto -

-end of translation -

As a sworn interpreter for the English language to the Berlin Judiciary, I hereby state and certify that the above translation is a true and complete translation of the German original document submitted to me.

This translation, comprising seven pages of text, does not contain the drawings of the original German document.



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